1. A semiconductor device comprising:

a substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween; and

a transistor gate over said substrate and between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, where said two second gate electrodes are provided on either side of said first gate electrode, and are separated from said first gate electrode by an insulating dielectric layer.

2. The device of claim 1, further comprising a conductive cap layer, said conductive cap layer electrically connecting the first and second gate electrodes.

3. The device of claim 2, wherein said first gate electrode comprises a metal and has a workfunction higher than that of said second gate electrodes.

4. The device of claim 2, wherein said first gate electrode is of N+ conductivity type and said second gate electrodes are of P+ conductivity type, and said device is over an n-well of said substrate.

5. The device of claim 2, wherein the first gate electrode is of P+ conductivity type and the second gate electrodes are of N+ conductivity type.

6. The device of claim 5, wherein the first and second gate electrodes comprise doped polysilicon.

7. The device of claim 5, wherein the first gate electrode comprises silicon-germanium.

8. The device of claim 5, wherein the first and second gate electrodes comprise a material selected from the group consisting of silicon-carbide and silicon-oxycarbide.

9. The device of claim 5, wherein the dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided oxide

10. The device of claim 9, wherein the dielectric layer is a nitride.

11. The device of claim 5, wherein each of said second gate electrodes occupy about 10% to about 33% of the total channel region length between said source/drain regions.

12. The device of claim 5, wherein the threshold voltages of said first and second gate electrodes are such that the portions of the channel region below said second gate electrodes are inverted first upon the application of a voltage to said conductive cap layer and the application of a greater voltage to said conductive cap layer is required to invert the portion of the channel region below said first gate electrode.

13. The device of claim 12, wherein said device is used in a DRAM.

14. The device of claim 13, wherein said device is used as an access transistor of said DRAM.

15. The device of claim 13, wherein said DRAM is part of a memory module.

16. The device of claim 12, wherein said device is part of an apparatus included in the group consisting of memory devices, logic devices, processor devices, and ASIC devices.

17. A semiconductor transistor having three gate electrodes, comprising:

a semiconductor substrate having at least two spaced doped source/drain regions, said at least two spaced doped source/drain regions defining a channel region therebetween;

a gate dielectric over said substrate;

a central gate electrode containing a first dopant provided over said gate dielectric and said channel region; and

two outer gate electrodes provided over said gate dielectric and said channel region and adjacent to said central gate electrode, said outer gate electrodes containing a second dopant having a different conductivity type than said first dopant and being separated from said central gate electrode by a dielectric layer;

wherein a workfunction difference between the central gate electrode and the outer gate electrodes is such that said central gate electrode experiences a greater threshold voltage than said outer gate electrodes.

18. The semiconductor transistor of claim 17, wherein at least a portion of the channel region below said outer gate electrodes is converted to a virtual source/drain junction upon the application of a voltage to the outer gate electrodes.

19. The semiconductor transistor of claim 18, further comprising a conductive cap layer, said conductive cap layer electrically connecting the central and outer gate electrodes.

20. The semiconductor transistor of claim 19, wherein said central gate electrode comprises a metal and has a workfunction higher that that of said outer gate electrodes.

21. The semiconductor transistor of claim 19, wherein said central gate electrode is of N+ conductivity type and said outer gate electrodes are of P+ conductivity type, and said transistor is over an n-well of said substrate.

22. The semiconductor transistor of claim 19, wherein the central gate electrode is of a P+ conductivity type and the outer gate electrodes are of an N+ conductivity type.

23. The semiconductor transistor of claim 22, wherein the central and outer gate electrodes comprise doped polysilicon.

24. The semiconductor transistor of claim 22, wherein the central gate electrode comprises silicon-germanium.

25. The semiconductor transistor of claim 22, wherein the central and outer gate electrodes comprise a material selected from the group consisting of silicon-carbide and silicon-oxycarbide.

26. The semiconductor transistor of claim 22, wherein the dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided oxide.

27. The semiconductor transistor of claim 26, wherein the dielectric layer is a nitride.

28. The semiconductor transistor of claim 22, wherein each of said outer gate electrodes occupy about 10% to about 33% of the total channel region length between said source/drain regions.

29. The semiconductor transistor of claim 22, wherein said transistor is part of a memory device.

30. The semiconductor transistor of claim 22, wherein said transistor is part of a DRAM.

31. The semiconductor transistor of claim 25, wherein said DRAM is part of a memory module.

32. The semiconductor transistor of claim 22, wherein said device is part of an apparatus included in the group consisting of logic devices, processor devices, and ASIC devices.

33. A semiconductor device, comprising:

a semiconductor substrate, said substrate having at least two separated doped source/drain regions;

three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity;

a gate dielectric separating said three gate electrodes from said substrate;

a thin dielectric layer separating said outer gate electrodes from said center gate electrode;

a conductive cap layer over said three vertical gate electrodes, said conductive cap layer electrically connecting said three vertical gate electrodes; and

insulating sidewalls adjacent to said conductive cap layer and said outer gate electrodes.

34. The semiconductor device of claim 33, wherein the three vertical gate electrodes comprise doped polysilicon.

35. The semiconductor device of claim 33, wherein the central gate electrode comprises silicon-germanium.

36. The semiconductor device of claim 33, wherein the three vertical gate electrodes comprise a material selected from the group consisting of silicon-carbide and silicon oxycarbide.

37. The semiconductor device of claim 33, wherein the dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided oxyide.

38. The semiconductor device of claim 37, wherein the dielectric layer is a nitride.

39. The semiconductor device of claim 33, wherein each of the outer gate electrodes occupy about 10% to about 33% of the total channel region length between said source/drain regions.

40. The semiconductor device of claim 33, wherein a workfunction difference exists between the central gate electrode and the outer gate electrodes.

41. The semiconductor device of claim 40, wherein said workfunction difference results in the central gate electrode having a higher threshold voltage than said outer gate electrodes.

42. A transistor structure comprising:

a semiconductor substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween;

a gate dielectric over said substrate;

a central gate electrode over said channel region and said gate dielectric; and

two outer gate electrodes over said channel region and said gate dielectric and adjacent to said central gate electrode, said outer gate electrodes being separated from said central gate electrode by a dielectric layer;

wherein a workfunction difference between the central gate electrode and the outer gate electrodes is such that said central gate electrode experiences a greater threshold voltage than said outer gate electrodes.

43. The transistor structure of claim 42, wherein at least a portion of the channel region of said substrate below said outer gate electrodes is converted to a virtual

source/drain junction upon the application of a voltage to the outer gate electrodes.

44. The transistor structure of claim 43, further comprising a conductive cap layer, said conductive cap layer electrically connecting the central and outer gate electrodes.

45. The transistor structure of claim 44, wherein said central gate electrode comprises a metal and has a workfunction higher that that of said outer gate electrodes.

46. The transistor structure of claim 44, wherein said central gate electrode is of N+ conductivity type and said outer gate electrodes are of P+ conductivity type, and said transistor structure is over an n-well of said substrate.

47. The transistor structure of claim 44, wherein the central gate electrode is of a P+ conductivity type and the outer gate electrodes are of an N+ conductivity type.

48. The transistor structure of claim 47, wherein the central and outer gate electrodes comprise doped polysilicon.

49. The transistor structure of claim 47, wherein the central gate electrode comprises silicon-germanium.

50. The transistor structure of claim 47, wherein the central and outer gate electrodes comprise a material selected from the group consisting of silicon-carbide and silicon-oxycarbide.

51. The transistor structure of claim 47, wherein the dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided oxide.

52. The transistor structure of claim 51, wherein the dielectric layer is a nitride.

53. The transistor structure of claim 47, wherein each of said outer gate electrodes occupy about 10% to about 33% of the total channel region length between said source/drain regions.

54. A processor system comprising:

a processor;

a memory device coupled to said processor, at least one of the memory device and processor comprising a transistor;

said transistor comprising:

a substrate, said substrate having at least two separated doped source/drain regions, said source/drain regions defining a channel region;

a gate dielectric over the substrate;

a central gate electrode over said gate dielectric and said channel region, said central gate electrode being of a first conductivity type;

two side gate electrodes, said side gate electrodes being on either side of said central gate electrode and over said gate dielectric and said channel region, said side gate electrodes being of a second conductivity type; and

a insulating dielectric layer separating said two side gate electrodes from said central gate electrode.

55. The processor system of claim 54, wherein said semiconductor transistor further comprises a conductive cap layer over the central gate electrode and the side gate electrodes, said conductive cap layer connecting said gate electrodes.

56. The processor system of claim 54, wherein said central gate electrode comprises a metal and has a higher workfunction than that of said side gate electrodes.

57. The processor system of claim 54, wherein said first conductivity tope is N+ type and said second conductivity type is P+ type, and said transistor is over an n-well of said substrate.

58. The processor system of claim 54, where said first conductivity type is P+ type and said second conductivity type is N+ type.

59. The processor system of claim 58, wherein when a voltage is applied to the conductive cap layer the portions of said channel region under the side gate electrodes become inverted to form virtual source/drain extensions.

60. The processor system of claim 59, wherein said central gate electrode and said side gate electrodes of said semiconductor transistor comprise doped polysilicon

61. The processor system of claim 59, wherein said central gate electrode and said side gate electrodes comprise silicon-carbide.

62. The processor system of claim 59, wherein said central gate electrode and said side gate electrodes comprise silicon-oxycarbide.

63. The processor system of claim 59, wherein the central gate electrode of said semiconductor transistor comprises silicon-germanium.

64. The processor system of claim 59, wherein the insulating dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided oxide.

65. The processor system of claim 64, wherein the insulating dielectric layer is nitride.

66. The semiconductor transistor of claim 59, wherein each of the side gate electrodes of said semiconductor transistor occupy about 10% to about 33% of the total channel region length between said source/drain regions.

67. The processor system of claim 59, wherein said semiconductor transistor further comprises an insulating layer over said conductive cap layer, said central gate electrode, and said side gate electrodes.

68. A method of forming a semiconductor transistor, comprising:

forming a first gate dielectric over a substrate;

forming a first type conductive gate region over said first gate dielectric;

forming a dielectric layer on the sides of said first type conductive layer;

forming a second gate dielectric over said substrate;

forming a second type conductive gate region over said second gate dielectric, adjacent to said dielectric layer, and on the sides of said first type conductive region; and

forming source and drain regions in said substrate to define a channel region between them and beneath said first and second conductive type gate regions.

69. The method of claim 68, wherein said first type conductive region is of P+ conductivity type and said second type conductive region is of N+ conductivity type.

70. The method of claim 69, wherein the act of forming said P+ type conductive region comprises:

forming said P+ type conductive region over said first gate dielectric;

forming a conductive material region over said P+ type conductive region;

forming a protective cap over said conductive material region; and

removing a portion of said P+ type conductive region, said conductive material region and said protective cap by etching, using said first gate dielectric as a stop to leave a freestanding vertical portion of said P+ type conductive region, said conductive material region and said protective cap.

71. The method of claim 70, wherein the act of forming said dielectric layer comprises forming a layer comprising a material selected from the group consisting of nitride, oxynitride, and nitrided oxynitride, on the sides of said P+ type conductive layer.

72. The method of claim 71, wherein the act of forming the N+ type conductive region comprises:

forming a region of N+ type conductive material over said second gate dielectric and adjacent to said dielectric layer and said P+ type conductive region; and

removing a portion of said N+ type conductive region to leave substantially vertical portions of said N+ type conductive region adjacent to and on the sides of said P+ type conductive region, wherein said dielectric layer separates said substantially

vertical portions of said N+ type conductive region from said P+ type conductive region.

73. The method of claim 72, further comprising forming a conductive cap over said substantially vertical portions of said N+ type conductive region and said P+ type conductive region.

74. The method of claim 73, further comprising forming electrically insulating sidewalls adjacent to said conductive cap and said substantially vertical portions of said N+ type conductive region.

75. The method of claim 74, further comprising performing an ion implant to form source and drain regions in said substrate.

76. The method of claim 75, wherein said P+ type conductive region is formed to a thickness of up to about 200 nm.

77. The method of claim 76, wherein said P+ type conductive region comprises doped polysilicon.

78. The method of claim 76, wherein said P+ type conductive region comprises silicon-germanium.

79. The method of claim 76, wherein said P+ type conductive region comprises silicon carbide.

80. The method of claim 76, wherein said P+ type conductive region comprises silicon oxycarbide.

81. The method of claim 75, wherein said dielectric layer is up to about 2.0 nm thick.

82. The method of claim 81, wherein said dielectric layer comprises nitride.

83. The method of claim 75, wherein said N+ type conductive region is up to about 50 nm thick.

84. The method of claim 83, wherein said N+ type conductive region comprises doped polysilicon.

85. The method of claim 83, wherein said N+ type conductive region comprises silicon carbide.

86. The method of claim 83, wherein said N+ type conductive region comprises silicon oxycarbide.

87. The method of claim 75, wherein said conductive cap is up to about 100 nm thick.

88. The method of claim 87, wherein said conductive cap comprises polysilicon.

89. A method of forming a semiconductor transistor, comprising:

providing a substrate;

forming a first gate dielectric layer over said substrate;

forming a P+ type conductive layer over said first gate dielectric;

selectively etching said P+ type conductive layer to leave at least two substantially vertical P+ type conductive layer regions over said first gate dielectric;

removing a portion of said first gate dielectric by selectively etching to said substrate to leave said at least two substantially vertical P+ type conductive layer regions over remaining said first gate dielectric;

forming a nitride layer on the sidewalls of said P+ type conductive layer;

forming a second gate dielectric over said substrate;

forming a N+ type conductive layer over said second gate dielectric and adjacent to said nitride layer and on the sides of each said substantially vertical P+ type conductive layer region;

etching said N+ type conductive layer to leave at least two structures, said at least two structures including the substantially vertical P+ type conductive layer regions and the adjacent regions of the N+ type conductive layer, said nitride layer separating said N+ type conductive layer regions from said P+ type conductive layer regions;

forming a conductive cap over each of said at least two structures;

forming insulating sidewalls adjacent to said N+ type regions and said conductive caps.

90. A method of forming a semiconductor transistor, comprising:

providing a substrate;

forming a first gate dielectric layer over said substrate;

forming a first gate electrode over said first gate dielectric layer, said first gate electrode having a first workfunction and sidewalls;

forming a dielectric layer on the sidewalls of said first gate electrode;

forming a second gate dielectric over said substrate;

forming a pair of second gate electrodes over said second gate dielectric and adjacent to said dielectric layer, said second gate electrodes being separated from said first gate electrode by said dielectric layer, said pair of second gate electrodes having a second workfunction which is different than said first workfunction;

forming a conductive cap over each of said gate electrodes; and

forming insulating sidewalls adjacent to said conductive cap and said gate electrodes.

91. The method of claim 90, wherein said second workfunction is more negative than said first workfunction.